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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/503,140	02/11/2000	Tsuneo Hayashi	SONY-T0130	6142

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/503,140	HAYASHI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,10-12,14-16,19,20 and 24-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,10-12,14-16,19,20 and 24-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on October 21, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Response to Amendment

2. Applicant's arguments with respect to amended claims 1-3, 5-7,10-12, 14-16, 19, 20 and 24-27 have been considered but are moot in view of the new ground(s) of rejection. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application

being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 19, 20 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Fuji, Hiroshi et al. (US 6392970 B1, hereafter referred to as Fuji).

4. 35 U.S.C. 102(e) rejection of Claims 1, 19 and 25.

Fuji teaches Prior Art whereby a reproducing light quantity control method for an optical memory device is used for a controlling means for controlling reading conditions while reading data from a recording medium (col. 2, lines 17-20, Fuji), comprising: an error correcting means for correcting errors in said read data (col. 2, lines 43-45, Fuji: Note: Fuji teaches that error rate is generally calculated using error correcting techniques); an error rate calculating means for calculating an error rate of said errors in said read data (col. 2, lines 43-45, Fuji); and a control means for controlling an amount of light from a laser diode used in reading said data (col. 2, lines 17-20, Fuji), or a frequency of a signal superimposed on a signal applied to the laser diode or an amplitude of the signal superimposed on the signal applied to the laser diode, based on the calculated error rate in order to reduce the error rate (col. 2, lines 35-42; Note: Fuji teaches that the error rate is required to determine the optimum reproducing light quantity, hence: Fuji teaches a control means for controlling an amount of light from a laser diode used in reading

said data based on the calculated error rate in order to reduce or minimize the error rate).

5. 35 U.S.C. 102(e) rejection of claim 20. See rejection to claims 1 and 19, above and Amplifier 22 in Fig. 6 in Fuji.

6. Claims 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine).

7. 35 U.S.C. 102(e) rejection of claim 10.

Takamine teaches a readout controlling apparatus for controlling reading conditions while reading data from a recording medium (see Fig. 33, Takamine), comprising: a reproducing means for reproducing data from a recording medium (see Optical Reader 5 in Fig. 33, Takamine); an error correcting means for correcting errors in said reproduced data (col. 25, lines 63-67, Takamine); an error rate calculating means for calculating an error rate (see Error Rate Measurement Unit 33 in Fig. 3, Takamine); and a control means for controlling a focus of light employed in reproducing said data (see Focus Controller 26 in Fig. 33,), based on the calculated error rate in order to reduce the error rate (see Abstract, Takamine).

8. 35 U.S.C. 102(e) rejection of claims 11 and 12.

Takamine teaches the use of CRC which is an error correcting techniques with the ability to correct errors but to also detect uncorrectable errors (col. 25, lines 63-67, Takamine). The Examiner would like to point out that that error rate consists of correctable as well as uncorrectable errors, i.e., all detectable errors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji, Hiroshi et al. (US 6392970 B1, hereafter referred to as Fuji) in view of Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine).

10. 35 U.S.C. 103(a) rejection of claims 2 and 3.

Fuji, substantially teaches the claimed invention described in claim 1 (as rejected above). In addition, Fuji teaches that bit error rate is generally calculated using error-correcting techniques (col. 2, lines 43-45, Fuji). The Examiner would like to point out that generally error correcting techniques not only have the ability to correct errors but to also detect uncorrectable errors and that error rate consists of correctable as well as uncorrectable errors, i.e., all detectable errors.

However Fuji, does not explicitly teach the specific use of a specific error correction technique that is capable of detecting uncorrectable errors to be added to the correctable errors in determining the bit rate.

Takamine, in an analogous art, teaches the use of CRC which is an error correcting techniques with the ability to correct errors but to also detect uncorrectable errors (col. 25, lines 63-67, Takamine). The Examiner would like to point out that error rate consists of correctable as well as uncorrectable errors, i.e., all detectable errors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fuji with the teachings of Takamine by including the specific use of an error correction technique that is capable of detecting uncorrectable errors to be added to the correctable errors in determining the bit rate. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that an error correction technique that is capable of detecting uncorrectable errors to be added to the correctable errors in determining the bit rate would provide the opportunity to calculate

the total detectable error rate (Note: error Rate is a standard calculation based on detectable errors).

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji, Hiroshi et al. (US 6392970 B1, hereafter referred to as Fuji) and Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine) in view of Lee, Woo-Nyun et al. (US 5930448 A, hereafter referred to as Lee).

12. 35 U.S.C. 103(a) rejection of claim 5.

Fuji and Takamine, substantially teach the claimed invention described in claims 1-3 (as rejected above). In addition, Fuji teaches that bit error rate is generally calculated using error-correcting techniques (col. 2, lines 43-45, Fuji). The Examiner would like to point out that product codes are a general error-correcting technique primarily used for recording mediums.

However, Fuji and Takamine, do not explicitly teach the specific use of Inner and outer code (see Fig. 1, Lee).

Lee, in an analogous art, teaches the specific use of Inner and outer code.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fuji and Takamine with the teachings of Lee by including use of Inner and outer codes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of readily available error correcting techniques

such as Inner and outer codes would provide the opportunity to calculate a bit error rate (see Fig. 3, Lee).

13. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji, Hiroshi et al. (US 6392970 B1, hereafter referred to as Fuji), Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine) and Lee, Woo-Nyun et al. (US 5930448 A, hereafter referred to as Lee) in view of Inoue, Sadayuki et al. (US 5696774 A, hereafter referred to as Inoue).

14. 35 U.S.C. 103(a) rejection of claim 6.

Fuji, Takamine and Lee substantially teach the claimed invention described in claims 1-5, 10-14, 19 and 20-22 (as rejected above). The Examiner would like to point out that error detection inherently requires various cumulative additions at the detector in order to detect errors when using parity codes. The Examiner would also like to point out that buffers or memory buffers are generally necessary in product codes since all the required operations for generating parity results for the two parity codes cannot be performed simultaneously, hence buffers are required to hold data until processing can be completed prior to submitting results to be used in calculating the BER.

However Fuji, Takamine and Lee do not explicitly teach the specific use of a buffer memory for cumulative addition results.

Inoue, in an analogous art, teaches Sixth and Seventh Memories 73 and 75 in Figure 24 of Inoue for storing results of cumulative additions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fuji, Takamine and Lee with the teachings of Inoue by including use of a buffer memory for cumulative addition results. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a buffer memory for cumulative addition results would provide the opportunity store data during intermediary steps inherently required by a decoder for parity data.

15. 35 U.S.C. 103(a) rejection of claim 7.

See rejection to claims 2 and 3, above.

16. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine) in view of Lee, Woo-Nyun et al. (US 5930448 A, hereafter referred to as Lee).

17. 35 U.S.C. 103(a) rejection of claim 14.

Takamine, substantially teaches the claimed invention described in claims 1-3 (as rejected above). The Examiner would like to point out that product codes are a general error-correcting technique primarily used for recording mediums.

However Takamine, does not explicitly teach the specific use of Inner and outer codes (see Fig. 1, Lee).

Lee, in an analogous art, teaches the specific use of Inner and outer codes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takamine with the teachings of Lee by including use of Inner and outer codes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of Inner and outer code would provide the opportunity to calculate a bit error rate (see Fig. 3, Lee).

18. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine) and Lee, Woo-Nyun et al. (US 5930448 A, hereafter referred to as Lee) in view of Inoue, Sadayuki et al. (US 5696774 A, hereafter referred to as Inoue).

19. 35 U.S.C. 103(a) rejection of claim 15.

Takamine and Lee substantially teach the claimed invention described in claims 1-5, 10-14, 19 and 20-22 (as rejected above). The Examiner would like to point out that error detection inherently requires various cumulative additions at the detector in order to detect errors when using parity codes. The Examiner would also like to point out that buffers or memory buffers are generally necessary in product codes since all the required operations for generating parity results for the two parity codes cannot be performed simultaneously, hence buffers are required to hold data until processing can be completed prior to submitting results to be used in calculating the BER.

However Takamine and Lee do not explicitly teach the specific use of a buffer memory for cumulative addition results.

Inoue, in an analogous art, teaches Sixth and Seventh Memories 73 and 75 in Figure 24 of Inoue for storing results of cumulative additions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takamine and Lee with the teachings of Inoue by including use of a buffer memory for cumulative addition results. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a buffer memory for cumulative addition results would provide the opportunity store data during intermediary steps inherently required by a decoder for parity data.

20. 35 U.S.C. 103(a) rejection of claim 16.

See rejection to claims 11 and 12, above.

21. Claims 24, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji, Hiroshi et al. (US 6392970 B1, hereafter referred to as Fuji) in view of Noguchi, Tatsumi et al. (US 5406429 A, hereafter referred to as Noguchi).

22. 35 U.S.C. 103(a) rejection of claims 24, 26 and 27.

Fuji, substantially teaches all the limitations of claims 24-27 (see rejection to claim 1, 19 and 20, above) except as noted below.

However Fuji, does not explicitly teach the specific use of controlling various other features such inclination, filter characteristics and speed.

Noguchi, in an analogous art, teaches adjusting parameters to optimize reproduction based on bit error rate (see Title and Abstract, Noguchi), which would encompass inclination, filter characteristics and speed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fuji with the teachings of Noguchi by combining the already existing error control signals based on error rate derived from an error correction technique taught in the Fuji patent to adjust additional parameters to optimize reproduction. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of controlling various other features such inclination, filter characteristics and speed would provide the opportunity optimize reproduction based on bit error rate.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakayama, Akihito et al. (US 6246041 B1) teaches a method for adjusting focusing characteristics of an optical pickup or an optical disc for recording and/or reproducing the optical disc. Nishiuchi, Kenichi et al. (US 6411592 B1) teaches a circuit and method for controlling the tracking operation using a bit error rate. Bakx, Johannes L. et al. (US 5471457 A) teaches an error-correction decoding algorithm is

switched between one used when a burst error has occurred, and one used when no burst error has occurred. Masaki, Takashi et al. (US 5392273 A) teaches a controller having a non-volatile memory stored with information for management of an optical storage drive. Kurz, Arthur et al. (US 5034939 A) teaches equipment for playing back and optionally also recording data that are read by an optical pick-up system by means of guiding a beam of light along the data-storage tracks of a rotating disk-shaped recorded medium and that are then decoded in a decoder that emits a pulse from its error output terminal for every bit error. Yoshimaru, Tomohisa et al. (US 4755980 A) teaches an optical disk on which information is recorded and reproduced by focused light and a recording/reproducing device for recording or reproducing information for the optical disk. YOSHIMARU, TOMOHISA (JP 61211840 A) teaches a means to correct a focus always to a proper position and to improve the error rate by converging a light from a light source onto a disc, changing a focus position, discriminating and storing the error rate at various focus position, discriminating the optimum focus position and setting the focus means to the focus corresponding to the result. HORIGOME, TOSHIHIRO (JP 08297849 A) teaches a control part that controls a light beam irradiated by an optical recording medium, such that the error rate is minimum according to the control information.

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
November 11, 2002

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